WHAT IS CLAIMED IS:

1. A multiple-gate transistor comprising:

a semiconductor fin formed in a portion of a bulk semiconductor substrate;

a gate dielectric overlying a portion of the semiconductor fin;

a gate electrode overlying the gate dielectric, the gate electrode having a bottom surface; and

a source region and a drain region formed in the semiconductor fin oppositely adjacent to the gate electrode, the source region having a source-substrate junction, and the drain region having a drain-substrate junction;

wherein the bottom surface of the gate electrode is lower than the source-substrate junction or the drain-substrate junction.

2. The structure of claim 1 wherein the gate electrode comprises polycrystalline or amorphous silicon.

3. The structure of claim 1 and further comprising a silicide region formed over the gate electrode.

4. The structure of claim 1 wherein the gate electrode is formed from a polycrystalline semiconductor.

5. The structure of claim 1 wherein the gate electrode is formed from a metallic nitride.

6. The structure of claim 1 wherein the gate electrode is formed from a metallic silicide.

7. The structure of claim 1 wherein the gate electrode is formed from a metal.

8. The structure of claim 1 wherein the gate electrode has a substantially planar top surface.

9. The structure of claim 1 and further comprising spacers on sides of the gate electrode.

10. The structure of claim 1 wherein the semiconductor fin comprises silicon.

11. The structure of claim 1 wherein the semiconductor fin comprises silicon and germanium.

12. The structure of claim 1 wherein the semiconductor structure further comprises an etchant mask overlying the semiconductor fin.

13. The structure of claim 1 wherein the semiconductor fin has a fin width that is larger at the top of the semiconductor fin than at the bottom of the semiconductor fin.

14. The structure of claim 1 wherein the gate dielectric comprises silicon oxide.

15. The structure of claim 1 wherein the gate dielectric comprises silicon oxynitride.

16. The structure of claim 1 wherein the gate dielectric comprises a high permittivity material.

17. The structure of claim 1 wherein the gate dielectric comprises a material selected from the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and zirconium oxide, and combinations thereof.

18. The structure of claim 1 wherein the gate dielectric comprises a material with a relative permittivity greater than about 5.

19. The structure of claim 1 wherein the gate dielectric has a thickness of between about 3 and about 100 angstroms.

20. The structure of claim 1 wherein the multiple-gate transistor is a triple-gate transistor.

21. The structure of claim 1 wherein the multiple-gate transistor is a double-gate transistor.

22. The structure of claim 1 wherein the multiple-gate transistor is an omega-gate transistor.

23. The structure of claim 1 wherein the bottom surface of the gate electrode is lower than the source-substrate junction and the drain-substrate junction by at least about 50 angstroms.

24. A method of forming a multiple-gate transistor, the method comprising:

providing a bulk semiconductor substrate;

forming a semiconductor fin in the bulk semiconductor substrate;

forming isolation regions on sides of the semiconductor fin;

forming a gate dielectric and a gate electrode on a portion of the semiconductor fin, the gate electrode having a bottom surface; and

forming a source region and a drain region in the semiconductor fin, the source region having a source-substrate junction and the drain region having a drain-substrate junction, the source-substrate junction or drain-substrate junction being higher than the bottom surface of the gate electrode.

25. The method of claim 24 wherein the source-substrate junction and the drain-substrate junction is higher than the bottom surface of the gate electrode by at least 50 angstroms.

26. The method of claim 24 wherein forming a semiconductor fin comprises:

forming a mask over the bulk semiconductor substrate; and

etching exposed regions of the semiconductor substrate to form the semiconductor fin.

27. The method of claim 26 further comprising removing the mask.

28. The method of claim 27 wherein the mask comprises a photoresist.

29. The method of claim 27 wherein the mask comprises a material selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride, and combinations thereof.

30. The method of claim 24 and further comprising strapping the source and drain regions with a conductive material.

31. The method of claim 24 and further comprising forming spacers on sides of the gate electrode.

32. The method of claim 24 and further comprising performing selective epitaxy on the source and drain regions.

33. The method of claim 24 wherein the semiconductor fin comprises silicon.

34. The method of claim 24 wherein the semiconductor fin comprises silicon and germanium.

35. The method of claim 24 wherein the gate dielectric comprises silicon oxide or silicon oxynitride or silicon nitride.

36. The method of claim 24 wherein the gate dielectric comprises a high permittivity material.

37. The method of claim 24 wherein the gate dielectric comprises a material selected from the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and zirconium oxide, and combinations thereof.

38. The method of claim 24 wherein the gate dielectric comprises a material with a relative permittivity greater than about 5.

39. The method of claim 24 wherein the gate dielectric has a thickness of between about 3 and about 100 angstroms.

40. The method of claim 24 wherein the gate electrode comprises polycrystalline or amorphous silicon.

41. The method of claim 24 wherein the gate electrode comprises poly-SiGe.

42. The method of claim 24 wherein the gate electrode comprises a metallic nitride.

43. The method of claim 24 wherein the gate electrode comprises a metallic silicide.

44. The method of claim 24 wherein the gate electrode comprises a metal.

45. The method of claim 24 wherein the multiple-gate transistor is a triple-gate transistor.

46. The method of claim 24 wherein the multiple-gate transistor is a double-gate transistor.

47. The method of claim 24 wherein the multiple-gate transistor is an omega-gate transistor.

48. A method of forming a semiconductor device, the method comprising:

providing a silicon substrate;

etching portions of the silicon substrate to form at least one semiconductor fin;

forming a gate dielectric layer over the semiconductor fin;

forming a gate electrode layer over the gate dielectric layer;

etching portions of the gate electrode layer to form a gate electrode, the gate electrode overlying sidewalls and a top surface of the semiconductor fin;

forming a region of material adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region of material; and

doping the sidewall of the semiconductor fin above the region of material.

49. The method of claim 48 wherein forming an isolation region comprises depositing an oxide material.

50. The method of claim 48 and further comprising forming a masking material over the silicon substrate and wherein the step of etching portions of the silicon substrate is performed in alignment with the masking material.

51. The method of claim 50 and further comprising removing the masking material after the semiconductor fin is formed.

52. The method of claim 50 wherein the gate dielectric layer and the gate electrode layer are formed over the masking material.

53. The method of claim 48 wherein forming a region of material comprises depositing a dielectric layer.

54. The method of claim 48 wherein forming a gate dielectric layer comprises forming a layer of a material with a relative permittivity greater than about 5.

55. The method of claim 48 and further comprising forming an isolation region adjacent the semiconductor fin.

56. The method of claim 48 and further comprising removing the region of material after doping the sidewall.